



PATENT ABSTRACTS OF JAPAN

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G06F 17/50**H01L 21/82****H01L 27/04****H01L 21/822**(21) Application number: **07329765**(71) Applicant: **HITACHI LTD**(22) Date of filing: **24.11.95**(72) Inventor: **ABE AKIO**(54) **CROSSTALK DELAY DECIDING METHOD AND
PARALLEL WIRING LENGTH LIMITING METHOD**path S1 and the parallel wiring length L_p .

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(57) Abstract:

PROBLEM TO BE SOLVED: To perform the desivation of parallel wiring length limit value and the delay calculation with high accuracy by adding the adjacency length to the crosstalk delay elements in the delay calculation.

SOLUTION: A erecti linear wiring (noticing path) S1 is prepared between a source gate 201 and a sink gate 202, and a wiring (adjacent path) S2 that is parallel to a part of the wiring S1 is prepared between a source gate 203 and a sink gate 204. The crosstalk delay value caused by an adjacent parallel wiring consisting of both paths S1 and S2 is calculated by simulation with the adjacency length L_s covering from the output point of the gate 201 of the path S1 through the start point of the adjacent parallel wiring and the parallel wiring length L_p of the adjacent parallel wiring as the parameter, and stored in a delay table while being made to correspond to the parameter. Then the object path S1 is selected, and the crosstalk delay value is found from the delay table using the adjacency length L_s of the

